REMARKS

This paper is submitted in reply to the Office Action dated July 27, 2006, within the three-month period for response. Reconsideration and allowance of all pending claims are respectfully requested.

In the subject Office Action, claims 31 and 32 were rejected under 35 U.S.C. § 101. Additionally, claims 1-27 and 31-33 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication No. 2003/0093655 to Grosior et al. (Grosior).

As an initial matter, Applicants wish to thank the Examiner for the courtesy extended in the telephonic interview between the Examiner and Applicants' representative on October 26, 2006. In the interview, conventional yield commands were disclosed in the context of the pending claims, and their absence in terms of the cited art. Proposed amendments to the claims to address the art-based rejections were discussed. More particularly, the Examiner suggested including additional claim language more particularly defining "yield commands." Based upon an understanding that a yield command includes (in terms of both the state of the art and the application as originally filed) relinquishing use by a thread/virtual processor of a CPU, the Examiner indicated that inclusion of such language would likely overcome the current rejections.

To this end, each independent claim (1, 13, 16 and 31) has been amended to include a yield command's function of relinquishing use of a multithreaded CPU by a first thread. Claim 31 has been further amended, and claim 32 has been cancelled to address the § 101 rejection. Applicants respectfully submit that no new matter is being added by the above amendments, as the amendments are fully supported in the specification, drawings and claims as originally filed.

As discussed above, claim 31 now recites a "tangible" medium, in deference to the Examiner. Applicants request the § 101 rejection be consequently withdrawn.

Next turning to the § 102(e) rejections, the rejected claims are generally directed to accommodating conventional yield calls for multithreaded CPU's by coordinating yielding threads. A yield command is an industry term of art referring to a convention whereby executing entities share access to single-threaded CPU's. When a thread

executes a yield, the yielding thread is suspended, i.e., relinquishes its use of the CPU, and the CPU is given to some other runnable thread. This thread typically idles until the CPU becomes available again. For instance, an idle executing entity, e.g., a virtual processor with no work to do, may relinquish its CPU availability in response to receiving a yield command from another executing entity with work to do.

Multithreaded CPU's generally provide greater processing efficiencies, but prior to the present invention, have been unable to use conventional yield commands. One reason for this is because multithreaded CPU's have a programmatic limitation that requires all threads to execute within a common virtual space, e.g., a hypervisor or partition. The claimed subject matter enables a thread executing on a multithreaded CPU to yield, and does so in a manner to ensure that all threads in the multithreaded CPU execute within the same virtual space. For instance, a single thread's yield may be deferred until another thread is in a ready-to-yield state, which ensures that the threads can all yield in a common virtual space.

Turning more particularly to the § 102(e) rejection of independent claim 1, this claim generally recites a method for sharing resources by enabling yield commands on a multithreaded CPU. The claimed invention specifically addresses programming constraints that have conventionally thwarted the use of yield commands on multithreaded CPU's. The claimed invention enables resource sharing using yield commands despite such constraints by deferring a yield comprising relinquishing use of the multithreaded CPU by a first thread executing on the multithreaded CPU, while waiting for at least a second thread executing on the multithreaded CPU to become ready to yield, and yielding the first thread in response to at least the second thread becoming ready to yield.

Applicants respectfully submit that Gosior fails to disclose or suggest the claimed yielding processes. Gosior makes no mention of a yield, in part, because of its disparate purpose. Gosior is directed towards improving "embedded" microprocessors [0009]. Gosior attempts to create efficiencies in embedded processors by using a pipeline technique that executes threads in parallel, staggered fashion [0021]. Significantly, the pipeline techniques do not disclose, motivate or suggest the claimed yield processes, e.g.,

relinquishing use of a CPU to another thread. Because at least this feature is neither disclosed nor suggested by the cited prior art, reconsideration and allowance of claim 1, as well as of claims 2-12 which depend therefrom, are respectfully requested.

Independent claim 13 recites deferring a yield comprising relinquishing use of the multithreaded CPU by a thread within a multithreaded CPU system while at least a subset of the plurality of threads yield, and abandoning the yield of the thread in response to detecting an event while the yield is deferred. As discussed above, Gosior fails to disclose or suggest a yield call, let alone deferring a yield. As such, Applicants respectfully request that the §102(e) rejection of claim 13 be withdrawn. Reconsideration and allowance of claim 1, as well as of claims 14 and 15 which depend therefrom, are respectfully requested.

Independent claim 16 is a computer hardware and software implementation that includes features similar to those recited in claim 1. These features include the yield processes that are neither taught nor suggested by Gosior Applicants consequently request reconsideration and allowance of claim 16, as well as of claims 17-22, 24-25 and 33 that depend therefrom.

Independent claim 31 is a program product implementation that includes features similar to those recited in claim 1. These features similarly include, among others, deferring a yield of a first thread executing on the multithreaded CPU. Since there is no such teaching present in Gosior, Applicants respectfully request reconsideration and allowance of claim 31.

As a final matter Applicants note that the Information Disclosure Statement mailed by Applicants on July 8, 2002 mentioned by Applicants in their Response of September 23, 2005 was inadvertently omitted. Applicants have now attached a copy of this submission and PTO/SB/08A along with a copy of the return postcard indicating the Office's receipt of same on July 15, 2002. Applicants respectfully request that the July 15, 2002 filing be included in the PAIR system image file wrapper file history and that the Examiner return initialed copies of all of the above-included PTO/SB/08A forms to Applicants in the Examiner's next communication.

In summary, Applicants respectfully submit that all pending claims are novel and non-obvious over the prior art of record. Reconsideration and allowance of all pending claims are therefore respectfully requested. If the Examiner has any questions regarding the foregoing, or which might otherwise further this case onto allowance, the Examiner may contact the undersigned at (513) 241-2324. Moreover, if any other charges or credits are necessary to complete this communication, please apply them to Deposit Account 23-3000.

Respectfully submitted,

October 27, 2006
Date

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